CLAIMS

1. A flash memory cell array, comprising: a substrate having an active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in rows above the active area, with the control gates being positioned above and aligned with the floating gates, select and erase gates aligned with and positioned on opposite sides of each of the stacked gates, a bit line above each row, bit line diffusions in the active area between and partially overlapped by two select gates, a bit line contact interconnecting the bit line and the bit line diffusions in each row, and a common source region in the active area beneath the erase gate and partially overlapped by the floating gates.

2. The flash memory cell array of Claim 1 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select and erase gates, and a second relatively thick dielectric between floating gates and control gates.

3. The flash memory cell array of Claim 1 wherein the control gates, select gates and erase gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during an erase operation.

4. The flash memory cell array of Claim 1 wherein the control gates, the erase gates, and the common source regions surround the floating gates in a manner which provides relatively large inter-gate and common source to floating gate capacitance for high-voltage coupling during program operation.

5. The flash memory cell array of Claim 1 wherein erase paths extend from the floating gates, through the tunnel oxide to the channel regions, and high voltage is coupled to the floating gates from the control gates, the select gates and the erase gates.

6. The flash memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and high voltage is coupled to the floating gates from the control gates, the erase gates on the sides of the stacked gates, and the common source regions.

7. The flash memory cell array of Claim 1 wherein the bit line for a row containing a selected cell to be programmed is held at 0 – 0.8 volt, a relatively low positive voltage is applied to a cell select gate for the selected cell, a relatively high positive voltage is applied to the source region, a relatively high positive voltage is applied to the erase gates, and a relatively high positive voltage is applied to the control gate in the selected cell.

8. The flash memory cell array of Claim 1 wherein an erase path is formed by applying a relatively high negative voltage to the control gates and a relatively low negative voltage to the select and erase gates, with the bit line diffusions, the source region and the active area at 0 volts.

9. The flash memory cell array of Claim 1 wherein an erase path is formed by applying a relatively low positive voltage to the control gates, the select gates and the erase gates, with the active area at a relatively high positive voltage and the bit line and source regions floating.

10. The flash memory cell array of Claim 1 wherein a read path is formed with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, the erase gates at near zero voltage, the select gates at relatively high positive voltage, and the control gate of a selected cell is biased at 0 - 2 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

11. The flash memory cell array of Claim 1 including an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

12. A process of fabricating a flash memory cell array, comprising the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, forming a first dielectric film over the silicon, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second silicon layer and the second dielectric film to form control, etching away portions of the first layer of silicon and the first dielectric film to form floating gates which are stacked beneath and self-aligned with control gates, forming source regions

in the active area of the substrate between the stacked gates, forming a third dielectric film on the side walls of the control and floating gates and on the active area of the silicon substrate, depositing a third silicon layer over the third dielectric film, removing portions of the third silicon layer to form select and erase gates on opposeite sides of the stacked gates, with the erase gates being positioned directly above the source regions, forming bit line diffusions in the active area of the substrate which are partially overlapped by the select gates, and forming bit line lines which extend above the gates and bit line contacts which interconnect the bit lines and the bit line diffusions.

13. A flash memory cell, comprising: a substrate having an active area, a vertically stacked pairs of floating gate and control gate above the active area, with the control gate being positioned above and aligned with the floating gate, select and erase gates aligned with and positioned on opposite sides of the stacked gates, a source region in the active area underneath the erase gate and partially overlapped by the floating gate, a bit line extending above the gates, a bit line diffusion in the active area partially overlapped by the select gate, and a bit line contact interconnecting the bit line and the bit line diffusion.

14. The flash memory cell of Claim 13 including a relatively thin tunnel oxide between the floating gate and the substrate, a first relatively thick dielectric between the floating gate and the select and erase gates, and a second relatively thick dielectric between the floating gate and the control gate.

15. The flash memory cell of Claim 13 wherein the control gate, the select gate and the erase gate surround the floating gate in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during an erase operation.

16. The flash memory cell of Claim 13 wherein the control gate, the erase gate, and the source region surround the floating gate in a manner which provides a relatively large inter-gate and source to floating gate capacitance for high-voltage coupling during a program operation.

17. The flash memory cell of Claim 13 wherein an erase path extends from the floating gate, through the tunnel oxide to the channel region, and high voltage

is coupled to the floating gate from the control gate, the select gate and the erase gate.

18. The flash memory cell of Claim 13 wherein a program path extends to the floating gate from an off-gate channel region between the select gate and the floating gate, and high voltage is coupled to the floating gate from the control gate, the erase gate, and the source region.

19. The flash memory cell of Claim 13 wherein a program path is formed by applying 0 – 0.8 volt to the bit line diffusions, a relatively low positive voltage to the select gate, a relatively high positive voltage to the source region, a relatively high positive voltage to the erase gate, and a relatively high positive voltage to the control gate.

20. The flash memory cell of Claim 13 wherein an erase path is formed by applying a relatively high negative voltage to the control gate and a relatively low negative voltage to the select and erase gates, with the bit line diffusion, the source region and the active at 0 volts.

21. The flash memory cell of Claim 13 wherein an erase path is formed by applying a relatively low positive voltage to the control gate, the select gate and the erase gate, with the active area at a relatively high positive voltage and the bit line and source regions floating.

22. The flash memory cell of Claim 13 wherein a read path is formed with the source region at 0 volts, the bit line diffusion at 1 - 3 volts, the erase gate near 0 volts, the select gate at relatively high positive voltage, and the control gate at 0 - 2 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

23. A process of fabricating a flash memory cell array, comprising the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, etching away portions of the first silicon layer to form spaced apart rows of silicon which extend in a first direction on the substrate, forming a first dielectric film over the silicon, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second silicon layer and the second

dielectric film to form control gates with exposed side walls which extend in a direction perpendicular to the rows of silicon, etching away portions of the rows of silicon and the first dielectric film to form floating gates which are stacked beneath and self-aligned with control gates, forming source regions in the active area of the substrate between the stacked gates, forming a third dielectric film on the side walls of the control and floating gates and on the active area of the silicon substrate, depositing a third silicon layer over the third dielectric film, removing portions of the third silicon layer to form select and erase gates on opposite sides of the stacked gates, with the erase gates being positioned directly above the source regions, forming bit line diffusions in the active area of the substrate which are partially overlapped by the select gates, and forming bit line lines which extend in the first direction above the gates and bit line contacts which interconnect the bit lines and the bit line diffusions.